17~~92~~. (Twice Amended) A memory system on a card that is connectable to a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and overhead data, and

means connectable to said computer system for controlling operation of the array, said controlling means including:

means responsive to receipt of a magnetic disk sector address from the host computer system for addressing a corresponding non-volatile memory sector,

means for reading the overhead data stored in the addressed sector <u>prior to either reading the user data from, or writing user data to, the addressed sector</u>, and

means responsive to the read overhead data for executing an instruction from the host computer system to perform a designated one of reading user data from, or writing user data to, the addressed sector.

23~~16~~. (Amended) A memory system [unit] having electrical terminations for establishing a connection with a host computer system, said memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of sectors that individually include a distinct group of said memory cells that are erasable together as a unit, the individual sectors having enough cells for storing a given amount of user data and some overhead data, and

a memory controller connected between said electrical terminations and said memory cell array for controlling operation of the array, said controller including:

means responsive to receipt of one or more mass memory storage block addresses through said terminations for addressing one or more of the non-volatile memory sectors, said addressing means including means responsive to an identification of any of the non-volatile memory

sectors that are unusable for substituting another usable sector therefor,

means for reading overhead data stored in the addressed sector prior to either reading the user data from, or writing user data to, the addressed sector, and

means responsive to the read overhead data for either reading user data from, or writing user data to, the addressed sector.

Add the following new claims:

~~--128.~~ 35. In a computer system including a processor and a memory system, wherein the memory system includes an array of integrated electronic circuit non-volatile floating gate memory cells partitioned into a plurality of distinct sectors of said memory cells that are individually erasable together as a unit separately from other sectors, a method of operating the memory system, comprising:

removably connecting said memory system including a controller to the computer system in a manner that said controller communicates with said processor for controlling operation of the array,

in response to receipt from the processor of an address in a format designating at least one mass memory storage block, generating through the controller (1) an address of at least one of said plurality of sectors of non-volatile memory corresponding to said at least one mass memory storage block and (2) an erase, write or read command,

in response to an erase command, erasing said at least one sector,

in response to a write command, reading, from an overhead portion of said at least one sector, overhead data of a characteristic of said at least one sector, and thereafter writing user data in the user data portion of said at least one sector and writing a characteristic of the written user data in the overhead portion of said at least one sector, and

in response to a read command, reading, from an overhead portion of said at least one sector, overhead data of a

characteristic of said at least one sector or of data stored in the user data portion of said at least one sector, and thereafter reading data from the user data portion of said at least one sector.

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~~129~~. The method of claim ~~128~~, which additionally comprises storing within the memory system links from addresses of any unusable sectors to addresses of others of said plurality of sectors, and wherein generating an address of said at least one of said plurality of sectors includes referring to said address links to substitute an address of a useable sector for an address of an unusable sector.

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~~130~~. The method of claim ~~129~~ the address links are stored for sectors that are unusable by reason of more that a predetermined number of memory cells therein being defective.

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~~131~~. The method of claim ~~129~~ wherein any links to addresses of useable ones of said plurality of sectors are stored in the overhead portion of unusable ones of said plurality of sectors.

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~~132~~. The method of claim ~~128~~ wherein erasing said at least one sector includes simultaneously erasing two or more but less than all of said plurality of sectors.

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~~133~~. The method of claim ~~128~~ wherein generating an address of said at least one sector includes generating addresses of a number of said plurality of sectors that is equal to a number of mass memory storage block addresses received from the processor.

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~~134~~. The method of claim ~~133~~, wherein the user data portion of the individual sectors has a capacity of substantially 512 bytes.

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~~135~~. The method of claim ~~128~~, wherein the overhead data stored in said overhead data portion of said at least one sector includes the address of said at least one sector.

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~~136~~. The method of claim ~~135~~, wherein, in response to either the write command or the read command, overhead data that is read includes the address of said at least one sector.

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~~137~~. The method of claim ~~136~~, wherein the address read from the overhead portion of said at least one sector is compared with the address that was generated through the controller.

45 ~~138~~. The method of claim 35 ~~128~~, wherein the overhead data stored in said overhead data portion of said at least one sector includes, if said at least one sector is defective, an address linking said at least one sector to another of said plurality of sectors.

46 ~~139~~. The method of claim 45 ~~138~~, wherein generating an address of said at least one of said plurality of sectors includes referring to said address linking to substitute an address of a useable sector for an address of an unusable sector.

47 ~~140~~. The method of claim 35 ~~128~~, wherein the overhead data stored in said overhead portion of said at least one sector includes an identification of any defective cells within the user data portion of said at least one sector.

48 ~~141~~. The method of claim 47 ~~140~~, additionally comprising, in response to either the write command or the read command, reading through the controller the identification of defective cells from the overhead portion of said at least one sector and then substituting therefore other cells within the said at least one sector.

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49 ~~142~~. The method of claim 35 ~~128~~, wherein the writing of a characteristic of the user data includes calculating an error correction code from the written user data and writing said error correction code into the overhead portion of said at least one sector.

50 ~~143~~. The method of claim 35 ~~128~~, wherein said at least one mass memory storage block sector address received from the processor includes a head, cylinder and sector.

9 ~~144~~. The method according to claim 1 ~~79~~, wherein causing the controller to generate an address of a non-volatile memory sector includes doing so for a non-volatile memory sector that corresponds to only one magnetic disk sector, wherein the user data portion of the individual non-volatile memory sectors has a capacity that is substantially the same as a user data portion of said one magnetic disk sector.--

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